FAST-SETTLING , LOW NOISE Ku BAND FUNDAMENTAL BIPOLAR VCO

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ABSTRACT:

This paper discusses fast-settling fundamental-output voltage-controlled oscillators in the Ku Band (15 to 18 GHz & 12 to 15 GHz), using silicon bipolar transistors and silicon varactor diodes. With these oscillators the output frequency settles within 2 μs to within $\pm$1 MHz of the final frequency. Phase noise at 16.2 GHz was measured to be -93 dBc/Hz at 100 kHz from the carrier.

INTRODUCTION:

Voltage Controlled Oscillators have been a key element for electronic warfare systems because of their fast switching, low power consumption and small size. Until now Ku-band fundamental VCOs have only been built using GaAs FETs[1]. It is well known that a GaAs FET oscillator is not only noisier, but also poorer in terms of switching time than a silicon bipolar transistor oscillator. Bipolar transistors have been used in push-push (second harmonic) configurations in Ku band VCOs[2]. However, such circuits have a number of disadvantages, such as spurious outputs at the fundamental frequency, the increased number of devices required and the complexity of the circuit compared to a fundamental oscillator.

A recently-developed high-performance silicon bipolar transistor[3] has now made it possible to realize bipolar VCOs with fundamental outputs of up to 18 GHz. Using a silicon-silicon technology, i.e. a silicon bipolar transistor and a silicon abrupt varactor diode, fast-settling, low-noise VCOs have been realized covering 12 to 15 GHz and 15 to 18 GHz.

In this paper we will discuss the device characterization, design approach for the VCO design, practical realization and measurement of the first Ku-band fundamental bipolar VCO.-

DEVICE CHARACTERIZATION:

The active device used for the oscillator is an Avantek-developed interdigitated arsenic-emitter Si bipolar transistor with 0.5 μm emitter width and 2 μm emitter-emitter pitch[3]. This device has 20 emitters with an emitter length of 15 μm, and a measured F_{max} of higher than 30 GHz. When biased at 10V, 20 mA the F_t and F_s (S21=0dB) were both approximately 10 GHz. MAG at 4 GHz was 16.7 dB and MUG at 18 GHz was 6 dB.

For tuning, a silicon abrupt varactor diode developed by Avantek was selected for its high-Q performance compared to commercially-available silicon abrupt diodes. With this diode, a Q of 5000 was measured at 50 MHz, with a capacitance ratio of 4.2 from 1 to 20 V.

OSCILLATOR DESIGN APPROACH:

A common-collector configuration was selected due to its inherent instability, minimum parasitics in the resulting circuit layout, and wider bandwidth capability compared to common-base or common-emitter circuits. Figure 1 shows the oscillator circuit.

The parallel compensating reactance shown in Fig. 2 is used to increase the oscillator bandwidth of a VCO[4]. It may be noted that the compensating reactance will be inductive or capacitive depending on the sign of input admittance of the oscillator device. Figure 2 shows the principle of operation of the compensating reactance. Using the small signal approach, the negative resistance analysis was done looking into the base of the device, with capacitive reactance on the emitter

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terminal. The capacitive series feedback and the bias circuits were optimized to generate the negative resistance in the desired frequency bands of 12 to 15 GHz and 15 to 18 GHz. Computer-aided design was used to analyze the oscillator circuit.

Next, the varactor circuit and the output circuit were modeled, combined into the oscillator circuit model, and optimized to achieve oscillation in the desired bands. Oscillation conditions[5] were analyzed using small signal S-parameter analysis. The output matching circuit is very lightly coupled in order to achieve low noise and to assure that the device will oscillate at the highest frequency possible. Although lighter coupling results in lower output power, it makes it possible to achieve higher frequency oscillations and wide bandwidth over the desired operating temperature range.

PRACTICAL REALIZATION:

The circuit discussed above was realized on a 10 mil alumina substrate. The bipolar transistor was operated at a bias of 9 Volts V_{ce} and I_e=16 mA. The capacitance required in the emitter circuit was realized using microstrip distributed capacitance, and the bias circuits were designed to cover the complete Ku band, without deteriorating the settling time performance of the oscillator. The abrupt varactor is an Avantek-developed diode with a Cj(4) of 0.5 pf. A reference voltage of -9 volt was used on the tuning diode, necessitating a bipolar tuning voltage.
To optimize the complete oscillator for practical output power, while maintaining bandwidth, a single-stage Ku-band GaAs FET amplifier is provided at the oscillator output. The amplifier stage uses a proprietary Avantek 0.5-µm GaAs FET, biased at 30 mA, with V_{ds} adjusted to 4.5 volts.

OSCILLATOR PERFORMANCE:

Two oscillators were required in order to cover the entire Ku band, the low-band oscillator tuning from 12 to 15 GHz and the high-band oscillator 15 to 18 GHz. Basic parameters of both the oscillators are given in the table below. Fig. 3 presents the detected power output vs. the tuning voltage for the high-band oscillator.

Parameter	Low Ku Band
Freq.Band	12 to 15 GHz
Min. Power	+6dBm
Pulling 2:1	14 MHz
Freq. Drift -54 to 75°C	< 240 MHZ
2n Harmonic	< -15 dBc

Parameter	High Ku Band
Freq.Band	15 to 18 GHz
Min. Power	+3dBm
Pulling 2:1	20 MHz
Freq. Drift -54 to 75°C	< 355 MHZ
2nd Harmonic	< -15 dBc

Modulation Sensitivity & settling time:

Modulation sensitivity over the band varied from 50MHz/V to 250MHz/V. The settling time was measured using the frequency counter method, and the downconverted frequency discriminator method. The oscillator frequency settling within +1 MHz was measured to be less than 2 µs as shown in fig.4

Phase Noise:

Oscillator phase noise was measured using the delay line discriminator technique. The results are shown in fig. 5, indicating a phase noise of-93 dBc at 100 kHz from carrier at 16.2 GHz.

ACKNOWLEDGEMENT:

The author is thankful to Bob Oyafuso for fruitful discussions and Jack Huynh for his craftsmanship in the fabrication and testing of the oscillators. The author acknowledges the work of C. Leung and R. Curby for the design of silicon bipolar transistor and silicon varactor diode respectively.

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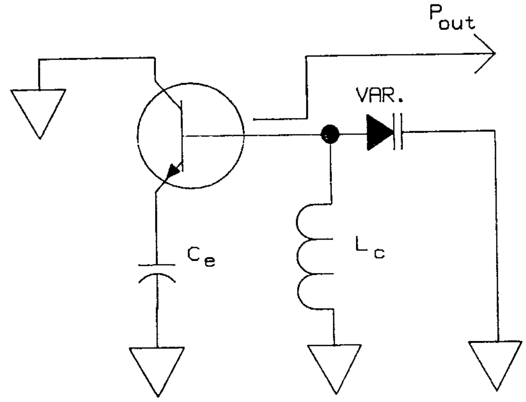

Fig. 1 Ku Band Bipolar VCO Configuration

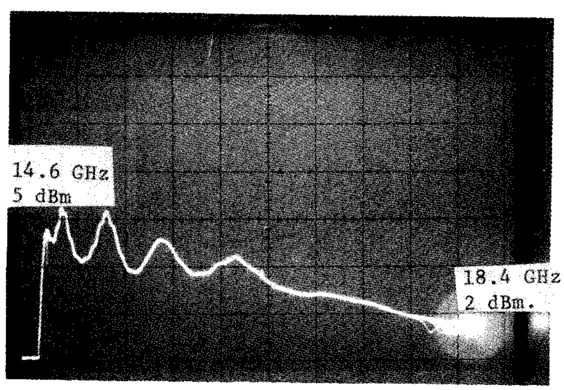

Fig. 3 High Band Frequency vs. Tuning Voltage

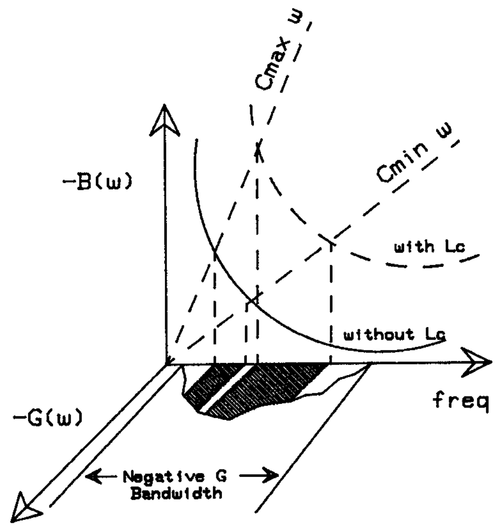

Fig. 2 Design Approach for a Wideband VCO

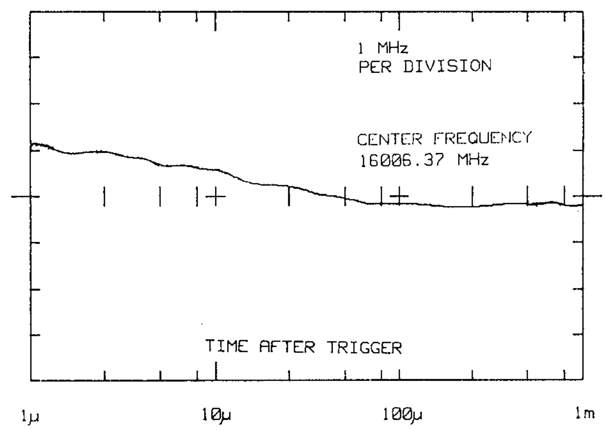

Fig. 4 Settling Time Plot for 14.3 GHz to 16 GHz

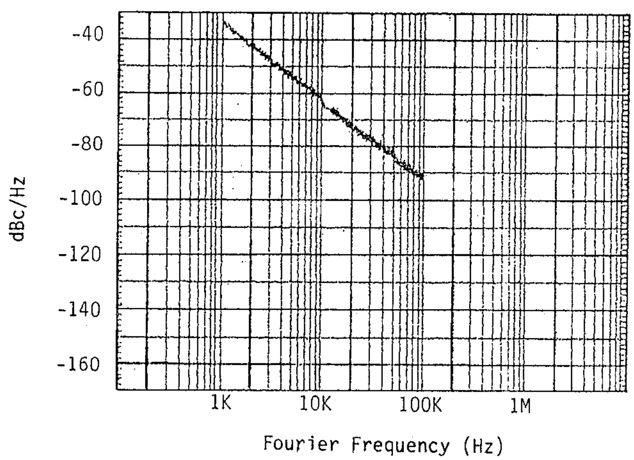

Fig. 5 Phase Noise at 16.2 GHz